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Charge Sharing- A Review

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Abstract—*For any A/D converters, the first thing that the converters need to do is to sample the time varying input signal. In CMOS technology, sampling is usually done with MOS switch and a sampling capacitor. Since various errors are associated with it and one of the most common is the charge injection which is discussed in this paper. Different approaches have been provided which minimizes the charge injection in switched current circuits. A topology for a CMOS charge pump has been discussed which exploits the charge injection phenomenon in MOS analog switches to obtain high precision.*

Keywords: *Analog-to-Digital Converters, Charge Sharing, CMOS, Sampler*

Introduction

All of us are known by the fact that most of the signals that are of practical interest such as speech, biological signals, radar signals and various communication signals such as audio and video signals are analog in nature. But these analog signals are first of all converted into digital signals for processing purposes because digital systems are considered to be more efficient and more reliable than analog processing. This procedure of converting the analog signal into the digital signal is called as the analog-to-digital conversion and this conversion is done in three steps: Sampling, Quantization and Coding [1]. Sampling function is performed with the help of the sampler (**sample and hold)** circuit which essentially consists of a switch and a capacitor. This sample and hold circuit works in two states: sample state and hold state. When the circuit is in "sample state", switch is closed and the voltage at input appears at the output. On the other hand when it is in "hold state", sampled voltage is held on the hold capacitor and the output is frozen at that point. Majority of these sample and hold circuits are implemented by making use of Metal Oxide Semiconductor transistor (MOST) technologies because MOST's are having very high input impedance which performs excellent holding functions. Sample and hold circuit with MOSFET as a switch is shown in figure 1, which essentially consists of two nodes i.e. signal source node and data storage node connected by a MOSFET. The major limitation to the accuracy of this circuit is the disturbance of the sampled voltage when the transistor is turned off. One cause is noise, which results in the random sequences of small perturbations. The other is the charge injection due to the carriers released from the channel. When the MOSFET is turned on, sampling function is preformed and when the switch is turned turned off, the data stored in the storage node will be held until the next operation step occurs. However, MOS switch is not an ideal switch. When the MOS switch conducts, a finite amount of mobile carriers are stored in the channel. When the transistor turns off, the channel charge disappears either through the source or drain terminals, creating an error component. A fraction of channel charge escapes to the substrate and this effect is called as the charge pumping.

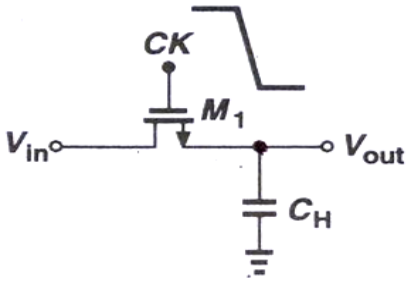

Fig. 1. Sample and hold circuit using MOSFET

Thus, in addition to the error that is caused as a result of the charge injection, there is another effect responsible for this error, and this effect is called as clock feed through [1]. For an NMOS device, negative charge is added to the sampled voltage as the MOS switch is turned off, causing a negative error voltage.

Charge injection phenomenon

Consider the circuit shown in figure 4 where N-MOSFET as the switch has been considered. When a positive voltage, whose magnitude is greater than the threshold voltage, is applied to the gate of the transistor, a channel of negative charges is created at the oxide-silicon interface of the transistor or in other words one can say that a conducting channel is formed under the MOS gate and the MOSFET is said to be in its on stat [2].

During this period i.e. in which the MOS switch is in its on state, the voltage across the sampling capacitor tracks the time varying input signal within the bandwidth and the charge in the channel at this instant is given by the equation:

$$Q_{ch} = WLC_{OX}(V_{DD} - V_{source} - V_{th}) \quad \text{.....(1)}$$

where:

$C_{OX} = \frac{\epsilon_{ox}}{t_{ox}}$ = capacitance per unit area of the gate oxide (F/ cm2)

V_{th} = threshold voltage

W = effective channel length

L = effective channel length

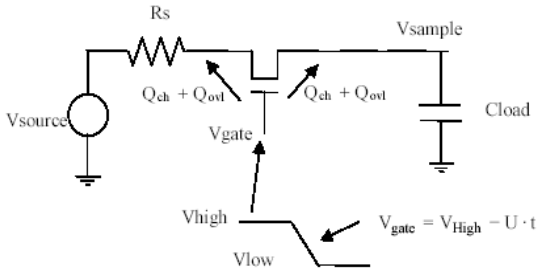

Fig 4. Sample and hold circuit used as a model for charge injection.

When the switch is turned off, charges that are present in the channel of the MOS switch will either flow to the input source or to the sampling capacitor. This phenomenon of sharing of charge between the source and the capacitor is called as the charge sharing or charge injection. As the gate voltage ramps down from V_{high}, mobile charge leaves the channel. This charge goes to either C_{load} or back to the source (input) and continues to evacuate the channel until the channel collapses at $V_{gate} = V_{source} + V_{thn}$ (subthreshold is ignored).When the channel collapses the second stage, clock feed through begins. During this stage, Vgate ramps from $V_{source} + V_{thn}$ to V_{low} and the overlap capacitance (C_{ol}) between the gate and drain continues to inject charge (Q_{ovl}) onto C_{load}. On the other hand, charges injected to the right side is deposited on capacitor (C_{load}) introducing an error in the voltage stored on the capacitor.

Assuming that half of the charge (Q_{ch}) is injected on the capacitor, in this case the resulting error voltage is given by:

$$\Delta V = \frac{WLC_{OX}(V_{DD} - V_{source} - V_{th})}{2C_{load}} \quad \text{..... (2)}$$

This error voltage limits the accuracy of the high performance analog CMOS circuits as they need large transistors (which invoke high channel charge) and small capacitors to reduce the transfer time constant In case of NMOS switch, the error given by the above equation appears in the form of a negative pedestal at the output as shown in the figure 5 [1].

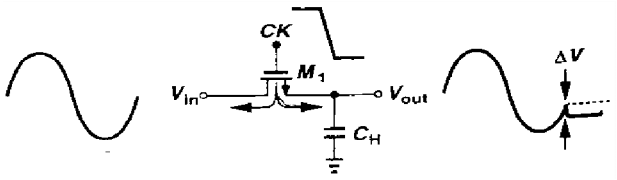

Fig 5. Effect of charge injection

The prediction of the error voltage ΔV will be based on the following qualitative physical description of the charge injection phenomenon in MOS transistor. A rapid variation of the gate voltage causes a variation of the surface potential as the amount of

mobile charges cannot change instantaneously. The surface potential induces an immediate variation of the depletion width, which compensates the excessive charge. Equilibrium corresponding to the new gate voltage is reached by the subsequent charge flow to drain and source. A fraction of charge in the channel escapes to the substrate leading to the charge pumping which is due to the recombination in the channel and into the substrate. Here the assumption has been made that half of the charge goes towards the source and half towards drain, but in reality, fraction of charge that exists through source and drain terminals is a relatively a complex function of various parameters such as impedance seen at each terminal to the ground and transition time of the clock. As a worst case, we assume that the entire channel charge is injected onto the sampling capacitor. Then based on the transition time of the clock, there exists two conditions: Fast switching off condition and slow switching off condition. In case of **fast switching off** condition, transistor conduction channel disappears very quickly. There is no enough time for the charge at the signal source side and the charge at the data holding side to communicate. Hence, percentage of charge injected into the data holding node approaches 50 percent, independent of the C_s/C_l ratio. On the other hand, in case of **slow switching off** conditions, communication between the charge at the signal source side and the charge at the data holding side is so strong that it tends to make the final voltages at both sides equal. This allows the majority of channel charge to go to the node with larger capacitance. The percentage of the channel charge injected into data holding node (when source resistance is infinitely large) has been plotted in figure 6 [3] [4].

Next is to see how charge injection affects the precision? Here two assumptions have been made:

a) $V_{in} = V_{out}$
b) all of the charge is deposited on the capacitor

Based on the above assumptions, sampled output voltage is expressed as:

$$V_{out} = \frac{V_{source} - WLC_{OX}(V_{DD} - V_{source} - V_{th})}{C_{load}} \quad \text{..... (3)}$$

Phase shift between input and output is neglected.

$$V_{out} = \frac{V_{source}(1+\frac{WLC_{OX}}{C_{load}}) - WLC_{OX}(V_{DD} - V_{th})}{C_{load}} \quad \text{,,,,, (4)}$$

The above equation suggests that the output deviates from the ideal value through two effects:

a) a non unity gain equal to $\left(1 + \frac{WLC_{OX}}{C_{load}}\right)$
b) a constant offset voltage equal to $\frac{-WLC_{OX}(V_{DD} - V_{th})}{C_{load}}$

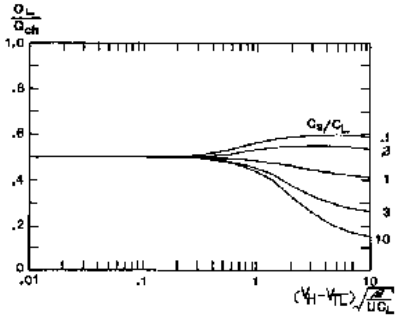

Fig 6. Percentage of channel charge injected into the data holding node corresponding to various C_s /C_l ratios

Since here it has been assumed that the channel charge is a linear function of input voltage, therefore, the circuit exhibits only gain error and d.c offsets shown in the figure 7

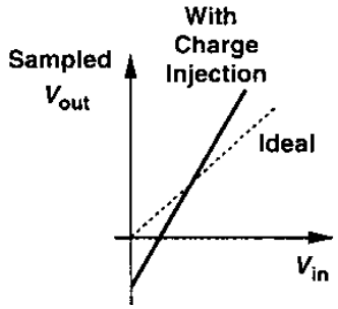

Fig 7. Input-output characteristics of sampling circuit in presence of charge injection

Charge leaking to the substrate

At long fall times (the switch-off time is longer than the channel transit time), nearly all the channel charge of the transistor is collected by the drain or source and even a low voltage V_{goff} does not change the amount of injected charge. The charge in the inversion layer follows the gate voltage variations. When the gate voltage reaches the threshold voltage, most of the channel charge has already been injected and the total injected charge Q_{inj} at the drain and source does not vary with V_{goff}. At short fall times, as the value of V_{goff} decreases, an increased amount of charge will flow into the substrate until the flat band voltage is reached. The charge that flows into the substrate reduces the total amount of injected charge at the drain and source. Beyond the flat band voltage, charge injection remains constant. The physical explanation is that when gate voltage V_g reaches threshold voltage V_{th}, most of the channel charge has not yet flown back to the drain and source. If we increase the value of V_g further, most of the mobile charges will be prevented from escaping to the substrate by the surface potential barrier and as V_{goff} is reduced, this barrier is progressively lowered. When the value of V_{goff} is approximately equal to flat band voltage, barrier is eliminated, saturation is reached and Q_{inj} is reduced.

Thus, we can say that when the gate off voltage is slightly smaller than the threshold voltage and fall time is longer than the channel transit time, in that case the substrate current is negligible.

Charge injection cancellation

Various methods have been employed to eliminate the effect of charge injections. Some of these methods have been described below:

A. Use of dummy device

In this case the charge injected by main transistor can be removed by means of second transistor as shown in the figure 8. In figure 8, M_2 is the dummy switch, driven by the clock, it is added to the circuit so that when M_1 turns off, and M_2 is turned on, channel charge deposited by the former on C_{load} is absorbed by the lattice to create a channel .Now, in order to ensure that the charge injected by M_1 i.e. Δq_1 is equal to that absorbed by M_2 i.e. Δq_2. Let us consider that half of the channel charge of $M_1$is injected into C_{load} i.e.

$$\Delta q_1 = \frac{W_1 L_1 C_{OX}(V_{ck} - V_{in} - V_{th1})}{2C_{load}} \quad (5)$$

Now,

$$\Delta q_2 = W_1 L_1 C_{OX}(V_{ck} - V_{in} - V_{th2})$$

Now $\Delta q_1 = \Delta q_2$, if and only if $W_2 = 0.5W_1$ and $L_2 = L_1$

But here the assumption of equal splitting of charge between source and drain has been made, which is generally invalid and hence making this approach less sensitive.

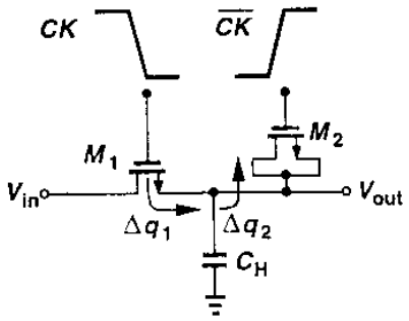

Fig 8. Addition of dummy device to reduce charge injection

B. Use of NMOS and PMOS

Another approach to lower the effect of charge injection includes both PMOS and NMOS devices i.e. making use of complementary transistors controlled by the complementary clock signals such that the opposite charge packets injected by the two cancel each other, as shown in figure 9.

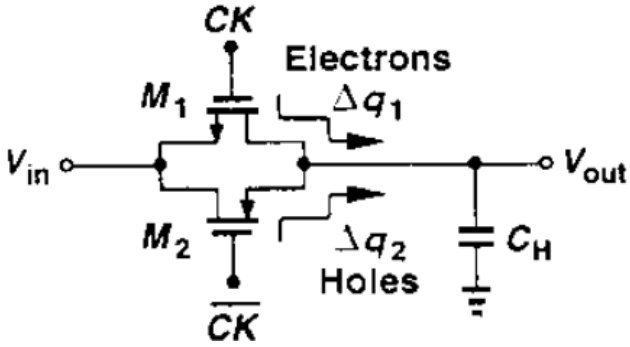

Fig 9. Use of complimentary switch to reduce charge injection

In this case for Δq_1 to cancel Δq_2, we must have:

$$W_1 L_1 C_{OX}(V_{ck} - V_{in} - V_{th}) = W_2 L_2 C_{OX}(V_{in} - |V_{thp}|) \quad (6)$$

This type of compensation is not very efficient, since it depends on the input voltage and no real matching exists between P and N channel transistors. Also the residual charge injection depends upon timing and skew of the two complimentary clocks, which may translate jitter into the amplitude noise.

C. Use of differential circuits

Third method that will eliminate the effect of charge sharing is by making use of differential circuits as shown in the figure 10. Here the charge injection appears as a common mode disturbance.

$$\Delta q_1 = WLC_{OX}(V_{ck} - V_{in1} - V_{th1})$$

$$\Delta q_2 = WLC_{OX}(V_{ck} - V_{in2} - V_{th2})$$

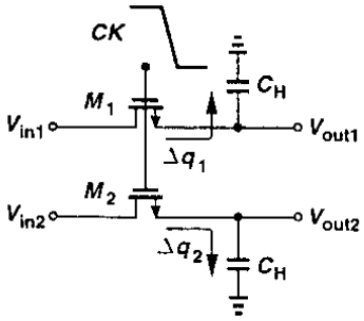

Fig 10. Differential sampling circuit

Over all error is not suppressed for differential signals but removes constant offset. Thus, various methods that are used in order to reduce the effects of the charge injection have been discussed. But to apply such cancellation techniques, usually device matching, multi phase clocks as well as extra bias signals may be required. However, there are certain techniques by means of which we can minimize the charge injection by removing the charge before the moment the charge injection could occur. One of such methods has been discussed below:

Principle of minimization of charge injection

There are certain techniques by means of which one can make the operation of circuit less sensitive to the charge injection by deviating the charge or part of it from the critical circuit node or in other words, reducing or eliminating the charge in the surface area before the clock switches its state. Figure 11 shows the basic switched current (SI) memory cell, which essentially consists of two MOST, N1 and N2.The output of N2 drives the gate of the transistor N1 [5] [6].

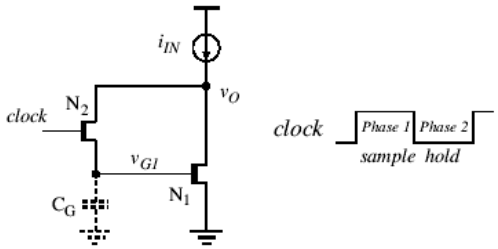

Fig 11. Basic scheme of switched current (SI) circuit

. Due to the charge injection in transistor N1, voltage variations of ΔV_{g1} at node V_{g1} will occur which in turn results in the current variations of Δin_1.This voltage variation is caused by an amount of charge, Δq, injected in the capacitor of the gate node. The principle of proposed minimization of charge injection does not aim at minimizing Δ_{Vg1} after it is generated, but at eliminating Δq. This Δq is related to the inversion layer of the MOS switch N2 at the end of the phase1. If the inversion layer is removed before phaes1 ends, no charge injection will take place MOS switch should be in good conducting state at first and then turned off before the clock changes its state to switch the operation phase or in other words we can say that gate-source voltage of N2 should be made strong at the beginning of the phase and reduced significantly when sampling is complete. For simplicity of controls of the circuit, the clock signal should have a uniformed voltage swing. A new circuit is therefore needed to generate a level variable gate voltage for the MOS switch without making the clock complex such a circuit is given in figure 12.

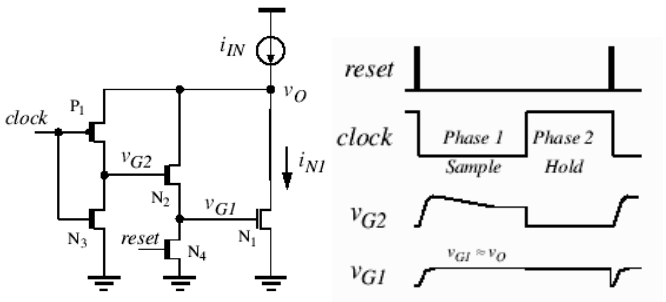

Fig 12. SI memory cell with the effect of charge injection minimized & waveforms the control signals & gate voltages.

In the circuit shown in figure 12, transistor N1 is the critical one, of which the gate node V_{g1} needs a protection from the switching noise including the charge injection, N2 is the switch that should be turned on to adjust V_{g1} to sample the input current. Voltage V_{g2} is made variable during the sample phase by means of transistor P1. Transistor N3 is used to pull V_{g2} down to zero volts during the second phase. Transistor N4 is turned on only at the beginning of each operation cycle to reset V_{g1} to zero volts.

A. Operation of the circuit

The operation of the circuit is divided into two phases:

Phase 1 (sample), clock = 0V and N3 is off: As the gate voltage V_{g1} is initially low, $i_{N1} << i_{IN}$ at the beginning of the phase. The voltage V_O increases quickly, raising V_{g1} and V_{g2}. Thus, both P1 and N2 are turned on so that V_{g1} and V_{g2} can be varied to adjust the current i_{N1}. When the level of the current i_{N1} becomes equal to that of i_{IN}, current of N2 and P1 approaches zero. In this case, if N2 is still on, then we have: Vo = V_{g1} and Vo < V_{g2}. In this situation, P1 has to have a current flowing from node V_{g2} to node Vo, which lowers the voltage V_{g2}. Two cases arise here:

a) V_{g2} = Vo
b) $V_{g2} = -V_{tp} >$ Vo

where: V_{tp} is the threshold voltage of P1.

In first case, current of P1 becomes equal to zero because V_{g2} – Vo, the voltage difference between the source and drain of P1 is reduced to zero. Second case arises when i_{N1} is a very weak and V_{g2} is very low. When V_{g2} is lowered to a level of $|V_{tp}|$, the current of P1 reduces to zero. Thus, V_{g2} can't be lowered to the level of Vo. In either of the two cases, the potential difference between V_{g2} and V_{g1} is not big enough for an inversion layer to exist in MOS switch N2 .Therefore, the inversion layer appearing at the beginning of the phase has been removed when V_{g2} is lowered.

Phase 2 (hold), clock = V_{dd} & P1 is off: Transistor N3 is turned on, discharging the capacitor at the gate of N2. This ensures the off state of N2.During this phase there, is no D.C path to the critical gate node Vg1. thus, the MOS switch N2 is turned on for the adjustment of the gate voltage V_{g1} to sample the input current, and the inversion layer of N2 is then removed so that there is a little charge to be injected when the operation phase changes. The state of the MOS switch N2 is controlled by the voltage V_{g2}.Two main elements contribute to the control of V_{g2}. First element is the current difference $\Delta i = i_{IN} - i_{N1}$ that determines when the transistor should be turned off i.e. V_{g2} being lowered during the first phase. Other one is the transistor P1 that had its gate voltage of zero volts and is used to provide a bidirectional connection between node Vo and V_{g2} during phase1. If $\Delta i > 0$, V_{g2} will be raised, by means of P1, for N2 to be driven on. If the current sampling is being completed, Δi approaches zero, i.e. little current flowing through P1 that is, however, still turned on because of the 0V at the gate. In this case, V_{g2} is automatically lowered to approach Vo, which reduces the gate-source of N2. Thus, during the sample phase, the removal of the inversion layer of the MOS switch N2 is done automatically after the input current is sampled.

Analytical model of error voltage

An analytical expression for the switch induced error voltage is derived by considering the circuit as shown in the figure (13). Using this expression one can explore the dependence of the error voltage on process and gate voltage falling rate. These results can be used to quickly predict the error voltage. Here we assume that the charge pumping phenomenon due to capture of the channel charges by the interface traps is not significant or we can say that when the transistor turns off, all the channel mobile charges exit through the source and drain ends [3].

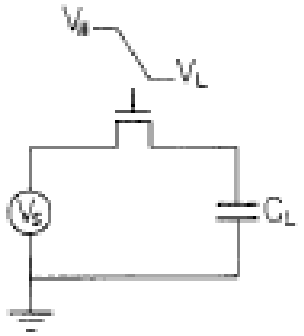

Fig 13. Schematic of the switch under study.

Total amount of switch induced error voltage on a switched capacitor is given by:

$$v_{dn} = -v_{dm} = -\sqrt{\frac{\pi U C_L}{2\beta}}\left(\frac{C_{ol} + \frac{C_{OX}}{2}}{C_L}\right)\text{erf}\left(\sqrt{\frac{\beta}{2UC_L}}V_{HT}\right) - \frac{C_{ol}}{C_L}(V_s + V_T + V_L)$$

$$V_{HT} = (V_H - V_S - V_T) \quad (7)$$

where:

v_{dn}= error voltage at the drain end after gate voltage V_G reaches V_L, U= gate voltage falling rate, v_{dm} = absolute value of v_{dn}, C_{ox} = gate capacitance, C_{ol} = gate-drain overlap capacitance, β= conductance coefficient, V_H = high value of V_G , V_S = signal voltage at source.

This switch-induced error voltage on a switched capacitor can be reduced by turning off the switch very slowly to allow the charges to return to the source end. Therefore, equation (7) can be simplified under two extreme cases [7]:

1) For slow switching off:

$$\frac{\beta V_{HT}^2}{2C_L} \gg U$$

$$V_{dm} = \left(\frac{C_{ol}+\frac{C_{OX}}{2}}{C_L}\right)\sqrt{\frac{\pi U C_L}{2\beta}} + \frac{C_{ol}}{C_L}(V_S + V_T - V_L) \quad (8)$$

2) For fast switching off:

$$\frac{\beta V_{HT}^2}{2C_L} \ll U$$

$$V_{dm} = \left(\frac{C_{ol}+\frac{C_{OX}}{2}}{C_L}\right) + \left(V_{HT} - \frac{\beta V_{HT}^3}{6UC_L}\right) + \frac{C_{ol}}{C_L}(V_S + V_T - V_L) \quad (9)$$

Dependence of switched induced error on process and electrical parameters

The switched induced error voltage on a switched capacitor is affected by many factors, which includes gate voltage falling rate, signal voltage level, substrate doping, oxide thickness, transistor size and source resistance of the signal voltage source. Here we will focus on the absolute value of this error voltage [8].

A. Dependence on gate voltage falling rate

Error voltage V_{dm} is plotted against the gate voltage falling rate ranging from104 V-s to1011V-s for four signal voltage levels 0, 1, 2 and 3 V, as show in the figure 14.

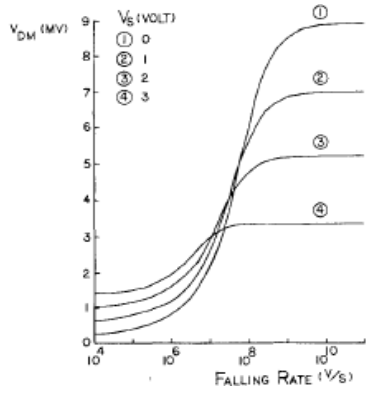

Fig 14. Error voltage as a function of gate voltage falling rate for four signal voltage levels.

In case of slow falling rate, most of the channel charge return to the source when the switch is on, and error voltage is due to clock feed through of the gate-drain overlap capacitance after the switch is turned off. At a very slow falling rate, V_{dm} saturates at $\frac{C_{ol}}{C_L}(V_S + V_T - V_L)$ .In case of fast falling rate, nearly one half of the channel charges are deposited in the storage capacitor and V_{dm} saturates at $\frac{V_{HT}\left(C_{ol}+\frac{C_{OX}}{2}\right)}{C_L} + \frac{C_{ol}}{C_L}(V_S + V_T - V_L)$.

B. Dependence on signal voltage level and substrate doping

Error voltage V_{dm} plotted against signal voltage V_S for five substrate dopings is shown in the figure 15. As the substrate doping increases, body effect increases accordingly. This in turn causes the threshold voltage in equation (7) to become more sensitive to V_S. The argument to the error function in expression (7) is smaller for large V_S or heavier substrate doping. As long as first term in (7) dominates e.g., at fast falling rates, V_{dm} is a strong function of V_S and more so in the heavy substrate doping circuits [9].

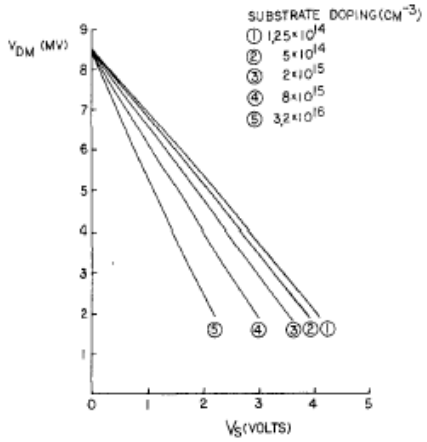

Fig 15. Error voltage as a function of signal voltage level for five substrate doping.

C. Dependence on oxide thickness

Advances in silicon technologies continue to make smaller MOS device dimensions possible. As the device size shrinks, the oxide thickness reduces, too. If storage capacitor oxide and gate oxide are scaled by the same factor, $\frac{\left(C_{ol}+\frac{C_{OX}}{2}\right)}{C_L}$ remains constant. The effect of C_L increase due to oxide reduction is exactly balanced by the effect of β increase (assuming constant W/L) such that the square root term and the error function term in equation (7) are unaltered. Hence, error voltage V_{dm} is not affected.

D. Dependence on Channel Width and Length

Transistor size is one of the most important variables in circuit design. Designers have to choose the appropriate combination of transistor sizes in order to achieve optimum circuit performance. Error voltage V_{dm} is plotted against channel length ranging from 1 to 10μm for four different channel widths 1, 4, 7 and 10 μm as shown in the figure 16. It is clear that smaller transistor size introduces smaller error voltage with the set of typical circuit parameter values.

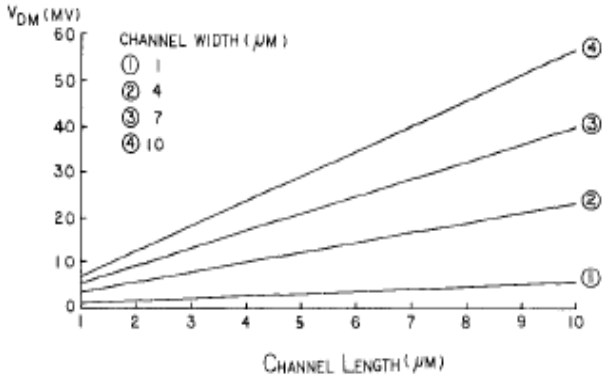

Fig 16. Error voltage as a function of transistor channel length for four channel widths..

E. Effect of Source Impedance

Source impedance of the signal voltage affects the error voltage. The circuit schematic which includes a source resistance is shown in figure 17.

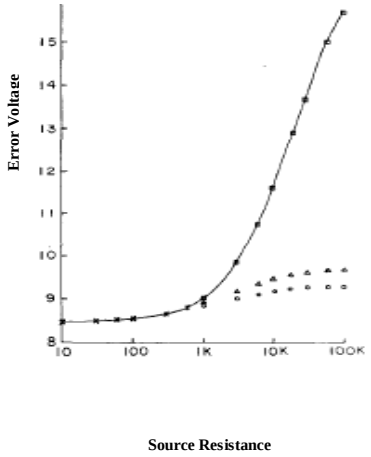

Fig 17. Error voltage as a function of source resistance.

Derivation of the analytical model including source resistance is quite similar to that without source resistance. Error voltage is plotted against source resistance in figure 17.As the source resistance increases, fewer channel charges return to the source end of the transistor and error voltage becomes larger.

Charge injection based CMOS charge pump

Here a new topology for a CMOS charge-pump has been described which exploits the charge injection phenomenon in MOS analog switches to obtain a high precision adjustable voltage without employing large capacitors. Since charge injection is considered as the source of error but here in this case (low-area low-power CMOS charge pump) charge injection phenomenon, instead of being a source of error, is exploited as the operation principle. The proposed circuit is particularly suitable to implement offset compensation schemes when area and power consumption constraints are stringent [6] [10].[11]

Circuit description

The charge-pump features three cascoded PMOS transistors (P0-P2) and three cascoded NMOS transistors (N0-N2) as shown in figure 18 [12].

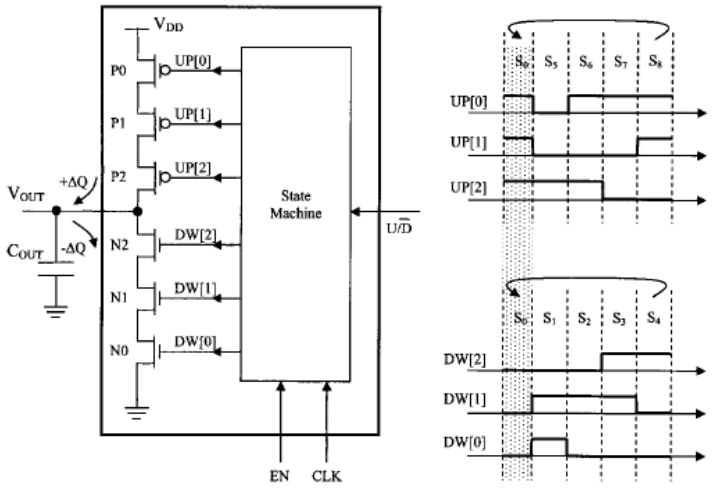

Fig 18. Charge pump block scheme

A state machine is used to generate the control signals UP[0:2] and DW[0:2] according to the waveforms depicted in figure 18 Starting from the reset state S0, to transfer a positive charge quantity +ΔQ from VDD to the output capacitor C_{OUT}, the state machine passes through the states S5 to S8 thus driving the upper PMOS devices with the signals UP [0:2]. The complementary signals DW [0:2] (states S1 to S4) are used to transfer a negative charge quantity –ΔQ from C_{OUT} to ground. In order to understand the operation of the circuit, transfer of a positive charge can be considered. During the first stage (state S5), the MOS switches P0-PI are turned on and the same charge Q_{ch} is stored in each inverted channel under the gate oxide, if both devices feature the same sizes. When the upper switch is turned off (state S6), its charge is injected into the power supply and into the capacitance of the drain node. It has been shown that, if the driving signal turns off quickly, the channel charge distributes fairly equally between the adjacent nodes [8].

Therefore, total charge which is transferred from the power supply is 3/2 Q_{ch} it holds:

$$Q_{ch} = W_p * L_p * C_{OX} * \left(V_{dd} - \left|V_{thp}\right|\right) \quad \text{..... (10)}$$

where:

$C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate capacitance/area and V_{thp} is the PMOS threshold voltage.

During next states (S7, S8) this charge is transferred to the output capacitor, thus obtaining a voltage step given by equation 11:

$$+\Delta V_{out} = +\frac{\Delta Q}{C_{out}} = \frac{3C_{out}}{2} \cdot \frac{1}{C_{out}} \quad \text{..... (11)}$$

The same expression holds for $-\Delta V_{out}$ and the area W_n and L_n of the NMOS device can be adjusted to compensate for the difference in the threshold voltages.

Second order charge injection errors

Since it has been found that due to the second order effects, the charge compensation is never ideal and residual charge injection error is still present. In order to study this effect, let us consider a widely used high speed, high precision sample and hold circuit as shown in the figure 19 [13].

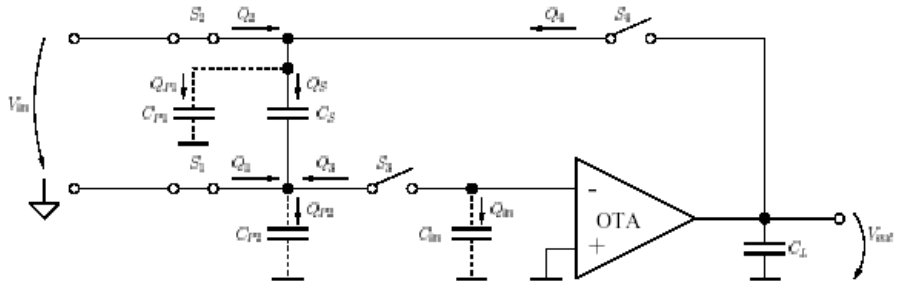

Fig 19. Sample and hold circuit

Let us consider the switching sequence S1 → S2 → S3 → S4 only. Our main goal here is to make Q1 = -Q3 in order to cancel the charge injection error term. Ideally, this would be obtained by sizing the switches $(W.L)_3 = 1/2(W.L)_1$. However, due to second order effects this cancellation is not exact.

There are several reasons for residual errors. Simple calculations as well as simulations indicate that the most important second order error source is due to the finite fall time of the clock edge t_0. Although the sum of the charges injected into the voltage source and the load capacitor remains constant, the charge is not equally partitioned but depends on the load. For a pure capacitive load the portioning can be calculated by:

$$\frac{Q_{inj,l}}{Q_{inj,l}+Q_{inj,r}} = \sqrt{\frac{\pi}{2} v \frac{C_L}{g_{DS}\, t_0}}\, \mathrm{erf}\left(\sqrt{\frac{1}{2v}\frac{g_{DS}\, t_0}{C_L}}\right) \qquad \ldots\ldots (12)$$

where:

$v = \left(\frac{V_{g,on}-V_{g,off}}{V_{g,on}-V_o-V_{th}}\right)$ and g_{DS} is the ON conductance of the switch[1].

Note from equation (12) that the influence of the fall time t_0 gets stronger for low resistive switches as applied in very fast sampling circuits. In this example, the charge distribution of S3 is unimportant since the both charges $Q_{inj,l}$ and $Q_{inj,r}$ are injected into the same node. However, the charge portioning has to be considered for switch S1.
For our high-speed sample and hold circuit the influence of the falling edge is significant. Hence, the injected charge Q1 depends on the load of switch S1 and choosing (W.L)3 = 1/2 (W.L)1 leads to a non-optimal compensation. Moreover, because of the on-resistance of switch S2 this load is not purely capacitive and, consequently, the injected charge is a function of this resistance as seen from figure 20.

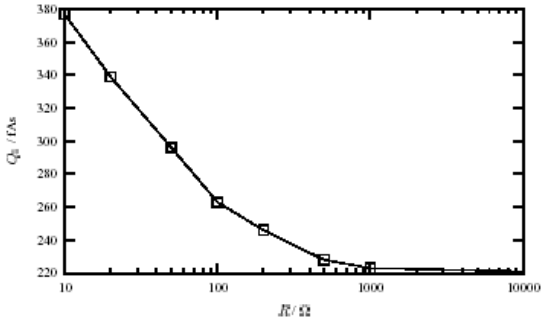

Fig 20. Injected charge Q1 as a function of on resistance of switch S2

But in most practical implementations, the on-resistance and hence the injected charge Q1 vary with the input signal resulting in a strong correlation between the input signal and the charge injection error. In these cases it is not sufficient to dimension $(W.L)_3$ or $(W.L)_1$ slightly different to compensate for the charge partitioning effect.

Conclusion

In analog-to-digital converters, we always use sample and hold circuit for sampling process. Sampling is done by MOS switches in case of CMOS circuits. Various errors associated with sampling process have been discussed in this paper. Various approaches that are being followed to minimize these errors have also been discussed.

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